



Errata: KS8695X Rev. B

Integrated Multi-Port Gateway Solution

Device: **KS8695X**
Revision: **B**
Date: **November 29, 2005**
Errata No.: **ERR8695X-112905**

No.	Description	Workaround
1	Packets that have patterns matching the Ethernet IP type field in their payloads at a 32 byte increment may be incorrectly identified as an IP packet. Since the packet will not have a correct IP checksum, it will be dropped. The probability of packet drop is very low.	Turn off hardware IP filtering functions.
2	For packets <49 bytes, IP header checksum is not generated	Use software to pad packets to at least 49 bytes in length.
3	8 or 16-bit External I/O Port Read Access Extra Cycles. The external I/O controller and the static memory controller (NOR Flash and SRAM) share the same data bus and an internal read buffer used by ARM AHB interface for data transfer. The read buffer is 32-bit wide and on every read operation the buffer is filled with 32 bits of data. Therefore for 8 or 16-bit port interfaces there will be multiple read cycles to fill the 32-bit buffer. This is acceptable for static memory since extra cycles are used to cache the data and are harmless. However, extra cycles can possibly have side effects for certain external I/O devices such as inadvertent clearing of a pending interrupt. This particular problem does not exist for 32-bit ports since every access completes in a single cycle.	<p>For the External I/O, every read from an 8-bit port must be presented as a 32-bit interface. The following steps implement this procedure:</p> <ol style="list-style-type: none">1. Program ERGCN (register offset 0x4020) bits [21:16] to 32-bit Data Width.2. S/W shift address by 2 bit position to left: A3A2A1A0=0000 → 0000, =0001 → 0100, =0010 → 1000, etc.3. H/W shift address bus by 2 bit position: A[21:0] → A[21:2]. See Figure 1 for illustration of system interface. <p>Every read from 16-bit port must be presented as 32-bit interface. Following steps implement this procedure:</p> <ol style="list-style-type: none">1. Program ERGCN (register offset 0x4020) bits [21:16] to 32-bit Data Width.2. S/W shift address by 1 bit position to left: A3A2A1A0=0000 → 0000, =0010 → 0100, =0100 → 1000, etc.3. H/W shift address bus by 1 bit position: A[21:1] → A[21:2]. See Figure 2 for illustration of system interface.



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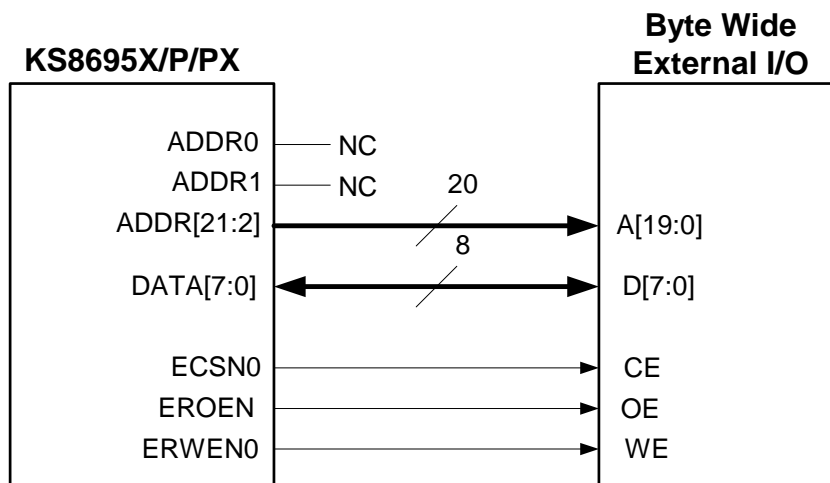


Figure 1 External I/O 8 bit system Interface

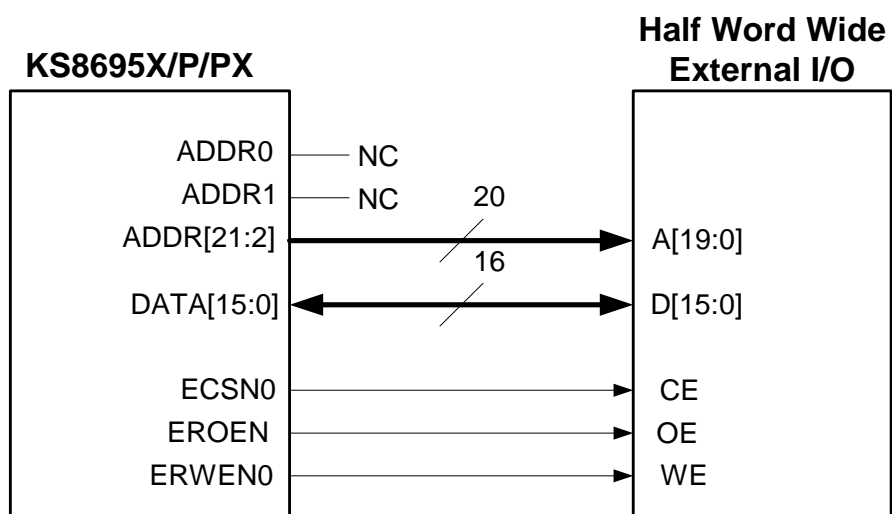


Figure 2 External I/O 16 bit system interface

Note: For the latest collateral update or any question regarding this Errata, please contact your local Salesperson or FAE.